Algorithm-Based Low-Power Transform Coding Architectures: The Multirate Approach

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***Abstract*—In most low-power VLSI designs, the supply voltage is usually reduced to lower the total power consumption. However, the device speed will be degraded as the supply voltage goes down. In this paper, we propose new algorithmic-level techniques to compensate the increased delays based on the multirate approach. We apply the technique of polyphase decomposition to design low-power transform coding architectures, in which the transform coefficients are computed through decimated low-speed input sequences. Since the operating frequency is M-times slower than the original design while the system throughput rate is still maintained, the speed penalty can be compensated at the architectural level. We start with the design of low-power multirate discrete cosine transform (DCT)/inverse discrete cosine transform (IDCT) VLSI architectures. Then the multirate low-power design is extended to the modulated lapped transform (MLT), extended lapped transform (ELT), and a unified low-power transform coding architecture. Finally, we perform finite-precision analysis for the multirate DCT architectures. The analytical results can help us to choose the optimal wordlength for each DCT channel under required signal-to-noise ratio (SNR) constraint, which can further reduce the power consumption at the circuit level. The proposed multirate architectures can also be applied to very high-speed block discrete transforms in which only low-speed operators are required.**

***Index Terms*— Discrete cosine transform, extended lapped transform, finite-precision analysis, low-power CMOS design, modulated lapped transform, multirate processing.**

I. Introduction

DUE to the limited power-supply capability of current battery technology, the power constraint becomes an important consideration in the design of personal communications services (PCS) devices. It has been shown that a reduction of the supply voltage is the leveraged way to lower the power consumption. However, a speed penalty is suffered for the devices (operators) as the supply voltage goes down. In [1], the techniques of "parallel processing" and "pipelining" were suggested to compensate the speed penalty, in which a simple comparator circuit was used to demonstrate how parallel independent processing of data can achieve good compensation at the architectural level. In most digital signal processing (DSP) applications, however, it is almost impossible to directly decompose the problems into independent and parallel tasks as in the comparator case. The properties of the DSP algorithms should be fully exploited in order to develop efficient compensation techniques to compensate the loss of speed performance under low-voltage operations. The main issue is to reformulate the DSP algorithms so that the desired outputs can be obtained at low-power consumption without hindering the system performance such as the data throughput rate. We call such an approach the *algorithm-based low-power design*.

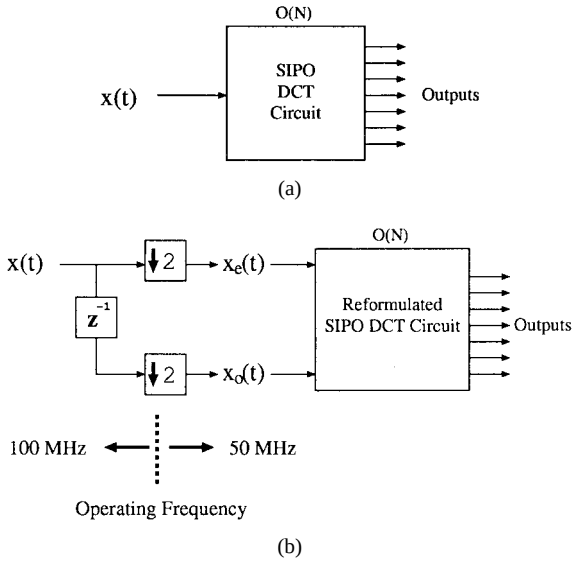

Fig. 1. (a) Original SIPO DCT circuit and (b) low-power DCT circuit using the multirate approach.

In this paper, we purpose a compensation technique—*the multirate approach*—to the design of low-power transform coding architectures at the algorithmic/architectural level. To motivate the idea, let us consider the discrete cosine transform (DCT) architecture in Fig. 1. For most of the existing serial-input–parallel-output (SIPO) DCT algorithms and architectures [2], [3], the processing rate must be as fast as the input data rate [Fig. 1(a)]. In our low-power design, the DCT is computed from the reformulated circuit using the decimated sequences [Fig. 1(b)]. Since the operating speed of the processing elements is reduced to half of the original data rate while the data throughput rate is still maintained, the speed penalty is compensated at the architectural level. As to the power consumption, using the CMOS power dissipation model [1], we can predict that the overall power consumption of the multirate design can be reduced to about one-third

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of the original system. Therefore, the downsampling scheme provides a direct and efficient way for the low-power design at the algorithmic/architectural level.

Two different approaches to derive the multirate low-power transform coding architectures are presented in this paper. One is the *polyphase decomposition approach*. By applying the technique of polyphase decomposition [4] to the infinite extent impulse response (IIR) transfer functions of discrete orthogonal transforms [3], we can reformulate the transfer functions so as to perform those transforms using M-times slower (where M is the decimation factor) decimated input sequences. The speed penalty caused by the low-voltage operation can be compensated at the architectural level at the expense of linear complexity increase. The other is based on the *logarithmic decomposition approach*. We show a scheme to perform the polyphase decomposition in a cascade way so that only $O(\log_2 M)$ overhead is required to compensate the speed penalty. We illustrate both low-power design approaches by using the DCT as examples. Later, the designs are extended to the modulated lapped transform (MLT) and extended lapped transform (ELT) [5], [6]. Then, based on the derivations of the MLT and ELT, we propose a unified low-power transform coding architecture. It can perform most of the existing discrete orthogonal transforms by simply reprogramming the computational modules.

At last, we examine the finite-wordlength effect of the proposed low-power DCT architectures. In general, shorter wordlength results in fewer switching events, lower capacitance, and shorter average routing length in the VLSI design. To achieve low power consumption at the circuit level, we need to choose minimum wordlength without degrading the signal-to-noise ratio (SNR) requirement. By applying our fixed-point analytical results, we can assign the optimal wordlength for each DCT channel under the SNR constraint. Moreover, the analyses show that the multirate designs have better numerical properties under fixed-point arithmetic.

The organization of this paper is as follows. In Section II, the derivation of the low-power DCT/IDCT algorithms and architectures are described. In Section III, we derive the multirate MLT and ELT algorithms and architectures. Then, a unified low-power IIR structure for most discrete orthogonal transforms is described. The fixed-point analysis is presented in Section IV followed by the conclusions.

II. Multirate Low-Power DCT/IDCT Architectures

The DCT of a series of input data starting from $x(t-N+1)$ and ending at $x(t)$ is defined as

$$X_{\mathrm{DCT},k}(t) = C(k)\sum_{n=0}^{N-1}\cos\left[(2n+1)\frac{k\pi}{2N}\right]x(t+n-N+1) \quad (1)$$

where $C(0) = \sqrt{1/N}$ and $C(k) = \sqrt{2/N}$, $k = 1, 2, \cdots, N-1$, are the scaling factors. By considering the transform operator as a linear shift invariant (LSI) system that maps the serial input data into the DCT coefficients, we can derive a second-order IIR transfer function from (1) as [3]

$$H_{\mathrm{DCT},k}(z) = \frac{X_{\mathrm{DCT},k}(z)}{X(z)} = \left((-1)^k - z^{-N}\right)\frac{C(k)\cos\omega_k\left(1-z^{-1}\right)}{1-2\cos 2\omega_k z^{-1}+z^{-2}} \quad (2)$$

where $\omega_k \triangleq k\pi/2N$; $X_{\mathrm{DCT},k}(z)$ and $X(z)$ denote the z-transforms of $X_{\mathrm{DCT},k}(t)$ and $x(t)$, respectively. For block processing, the z^{-N} in (2) can be eliminated. The corresponding IIR DCT structure is shown in Fig. 2. It works in a SIPO way, and the resulting parallel architecture is regular, modular, and fully pipelined. Also, the SIPO feature avoids the input buffers as well as the index mapping operations that are required in most parallel-input–parallel-output (PIPO) DCT architectures [7], [8]. One disadvantage of the IIR structure in Fig. 2 is that the updating of the DCT coefficients must be as fast as the input data rate. Hence, it suffers from the speed penalty as the supply voltage of the computational module goes down for low power consumption. We shall reformulate the transfer function using the multirate approach, so that speed degradation can be compensated at the architectural level.

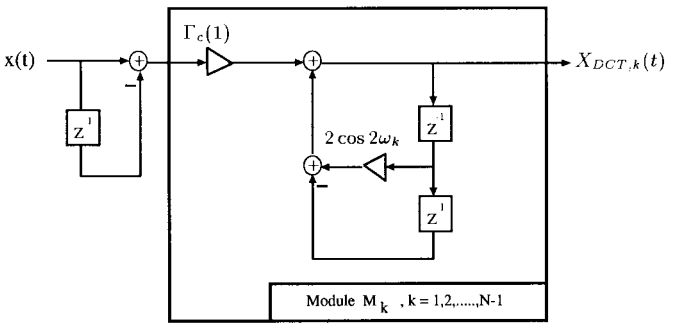

Fig. 2. IIR DCT architecture, where $\Gamma_c(m) \triangleq (-1)^k C(k)\cos m\omega_k$. For $k = 0$, the $X_{\mathrm{DCT},0}(t)$ can be computed using a simple accumulator.

A. Low-Power Design of the IIR DCT

Splitting the input data sequence into the *even* sequence, $x_e(t, n) = x(t + 2n - N + 1)$, $n = 0, 1, \cdots, N/2-1$, and the *odd* sequence, $x_o(t, n) = x(t + 2n - N + 2)$, $n = 0, 1, \cdots, N/2-1$, (1) becomes

$$X_{\mathrm{DCT},k}(t) = C(k)\sum_{n=0}^{N/2-1}\cos\left[(4n+1)\frac{k\pi}{2N}\right]x_e(t,n) + C(k)\sum_{n=0}^{N/2-1}\cos\left[(4n+3)\frac{k\pi}{2N}\right]x_o(t,n). \quad (3)$$

Taking the z-transform on both sides of (3) and rearranging, we have

$$X_{\mathrm{DCT},k}(z) = \frac{C(k)\left((-1)^k - z^{-N/2}\right)}{1-2\cos 4\omega_k z^{-1}+z^{-2}} \times\Big(\left[X_e(z)-X_o(z)z^{-1}\right]\cos 3\omega_k + \left[X_o(z)-X_e(z)z^{-1}\right]\cos\omega_k\Big) \quad (4)$$

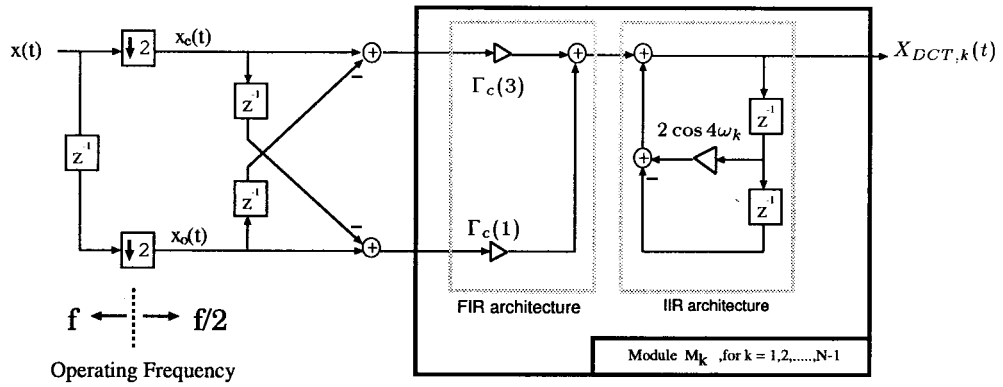

Fig. 3. Low-power polyphase IIR DCT architecture with $M = 2$.

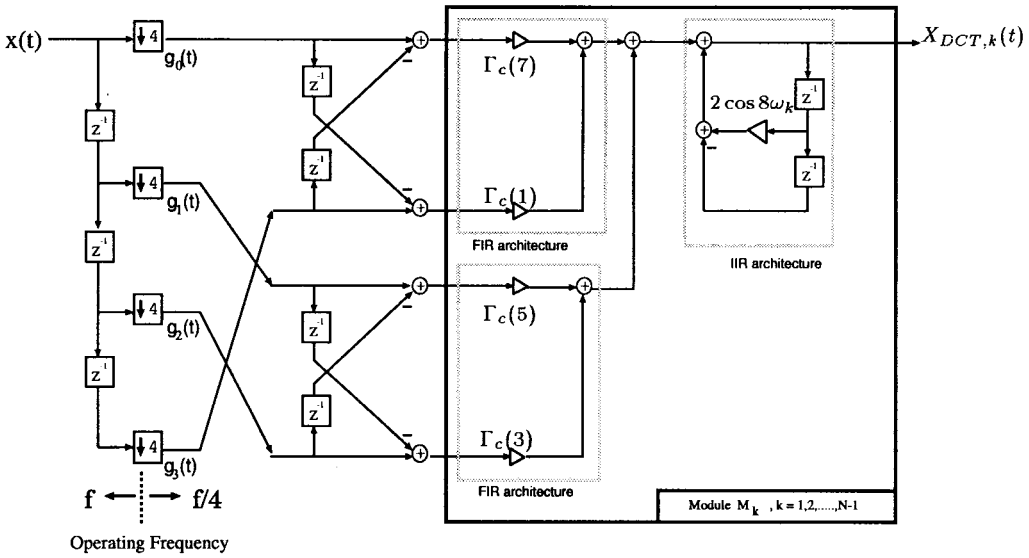

Fig. 4. Low-power polyphase IIR DCT architecture with $M = 4$.

where $X_e(z)$ and $X_o(z)$ are the z-transforms of $x_e(t, n)$ and $x_o(t, n)$, respectively. The parallel architecture to realize (4) is depicted in Fig. 3.

To achieve downsampling by the factor of four, we can split the input data sequence into four decimated sequences $g_i(t, n) \triangleq x(t + (4n + i) - N + 1), i = 0, 1, 2, 3,$ for $n = 0, 1, \cdots, N/4 - 1$. Following the derivations in (3) and (4), we can write $X_{\mathrm{DCT},k}(z)$ as

$$\begin{aligned} X_{\mathrm{DCT},k}(z) = \frac{C(k)((-1)^k - z^{-N/4})}{1 - 2\cos 8\omega_k z^{-1} + z^{-2}} \\ \times([G_0(z) - G_3(z)z^{-1}]\cos 7\omega_k \\ + [G_1(z) - G_2(z)z^{-1}]\cos 5\omega_k \\ + [G_2(z) - G_1(z)z^{-1}]\cos 3\omega_k \\ + [G_3(z) - G_0(z)z^{-1}]\cos \omega_k) \end{aligned} \quad (5)$$

where $G_i(z)$ is the z-transform of $g_i(t, n)$. The corresponding multirate architecture is shown in Fig. 4.

From Figs. 3 and 4, we can see that basically the multirate DCT architectures retain all advantages of the original IIR structure in [3] such as modularity, regularity, and local interconnections. This makes the proposed architectures very suitable for VLSI implementations. It is also interesting to see that the speed-compensation capability of our architectures is achieved at the expense of "locally" increased hardware complexity and routing paths. This feature of local interconnection and local hardware overhead is especially preferable in VLSI design when the transformation size is large (e.g., the MPEG audio codec in which a 32-point DCT/IDCT is used [9]).

B. Low-Power Design of the IIR IDCT

The IIR transfer function for the IDCT is given by [3]

$$\begin{aligned} H_{\mathrm{IDCT},n}(z) = \frac{(-1)^n C(1)\sin \omega_n}{1 - 2\cos \omega_n z^{-1} + z^{-2}} \\ + (C(0) - C(1))z^{-(N-1)} \end{aligned} \quad (6)$$

where $\omega_n \triangleq ((2n + 1)/2N)\pi$. As with the derivations of the low-power IIR DCT, the multirate transfer function for the IDCT with $M = 2$ can be derived as

$$\begin{aligned} X_{\mathrm{IDCT},n}(z) = \frac{(-1)^n C(1)}{1 - 2\cos 2\omega_n z^{-1} + z^{-2}} \\ \times (X_e(z)\sin 2\omega_n + (1 + z^{-1})X_o(z)\sin \omega_n) \\ + (C(0) - C(1))z^{-(N-1)}X(z). \end{aligned} \quad (7)$$

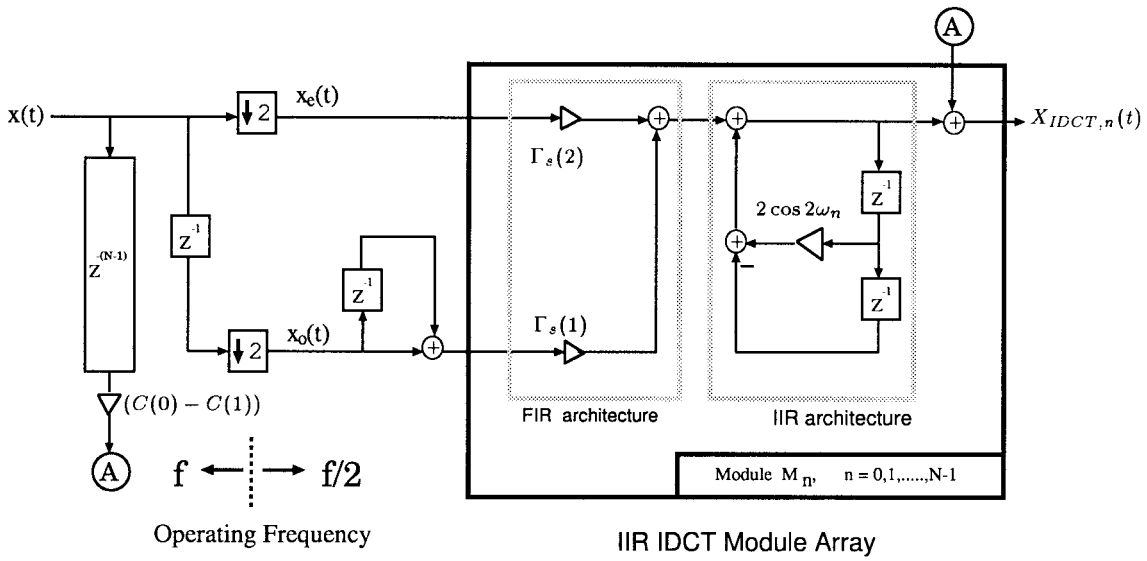

Fig. 5. Low-power polyphase IIR IDCT architecture with $M = 2$, where $\Gamma_s(m) \triangleq (-1)^n C(1) \sin m\omega_n$.

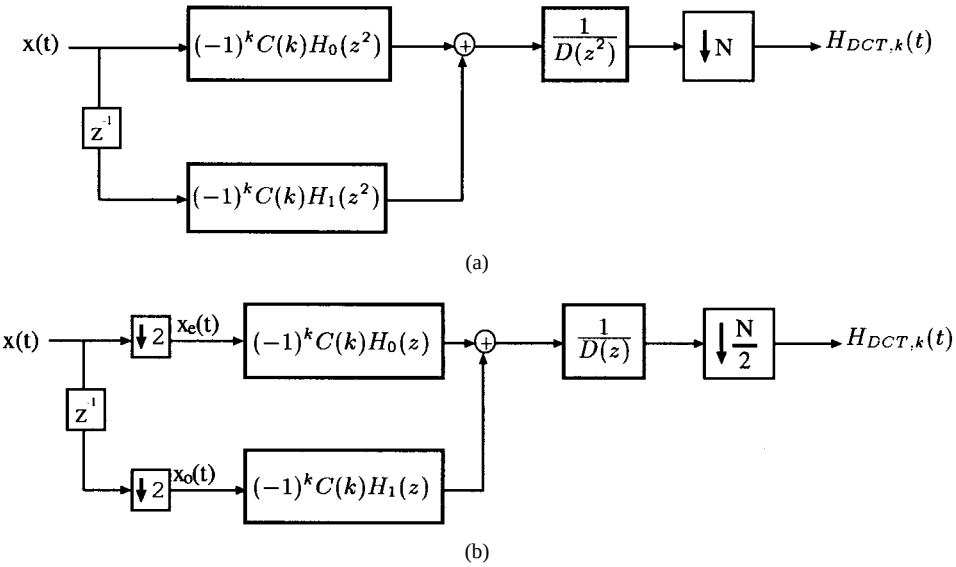

Fig. 6. (a) Polyphase representation of $H_{\mathrm{DCT},k}(z)$ and (b) polyphase representation of $H_{\mathrm{DCT},k}(z)$ after applying the noble identity.

The corresponding low-power IIR IDCT structure is illustrated in Fig. 5. Similarly, the multirate transfer function for $M = 4$ can be derived as

$$\begin{aligned} X_{\mathrm{IDCT},n}(z) &= \frac{(-1)^n C(1)}{1 - 2\cos 4\omega_n z^{-1} + z^{-2}} \\ &\times \big(G_0(z)\sin 4\omega_n + \big[G_1(z) + G_3(z)z^{-1}\big]\sin 3\omega_n \\ &+ \big(1 + z^{-1}\big)G_2(z)\sin 2\omega_n + \big[G_3(z) + G_1(z)z^{-1}\big] \\ &\times \sin\omega_n\big) + \big(C(0) - C(1)\big)z^{-(N-1)}X(z). \end{aligned} \tag{8}$$

C. Polyphase Decomposition Approach

In the preceding discussions, we derived the multirate DCT/IDCT by rearranging the z-transforms of the decimated sequences. Here, we will show a systematic way to derive the results by applying the *polyphase decomposition* [4] to the original IIR transfer function.

Substitute the identity that

$$\frac{1}{1 - 2\cos 2\omega_k z^{-1} + z^{-2}} = \frac{1 + 2\cos 2\omega_k z^{-1} + z^{-2}}{1 - 2\cos 4\omega_k z^{-2} + z^{-4}} \tag{9}$$

into the IIR DCT transfer function in (2). After rearranging, $H_{\mathrm{DCT},k}(z)$ under block processing can be written as

$$H_{\mathrm{DCT},k}(z) = \frac{(-1)^k C(k)}{D(z^2)}\big[H_0(z^2) + z^{-1}H_1(z^2)\big] \tag{10}$$

where $D(z^2) = 1 - 2\cos 4\omega_k z^{-2} + z^{-4}$, $H_0(z^2) = \cos\omega_k - \cos 3\omega_k z^{-2}$, and $H_1(z^2) = \cos 3\omega_k - \cos\omega_k z^{-2}$, and its corresponding polyphase implementation is shown in Fig. 6(a). Then we can apply the *noble identities* [4] to distribute the downsampling operation toward the left and obtain Fig. 6(b), which leads to the multirate DCT architecture in Fig. 3.

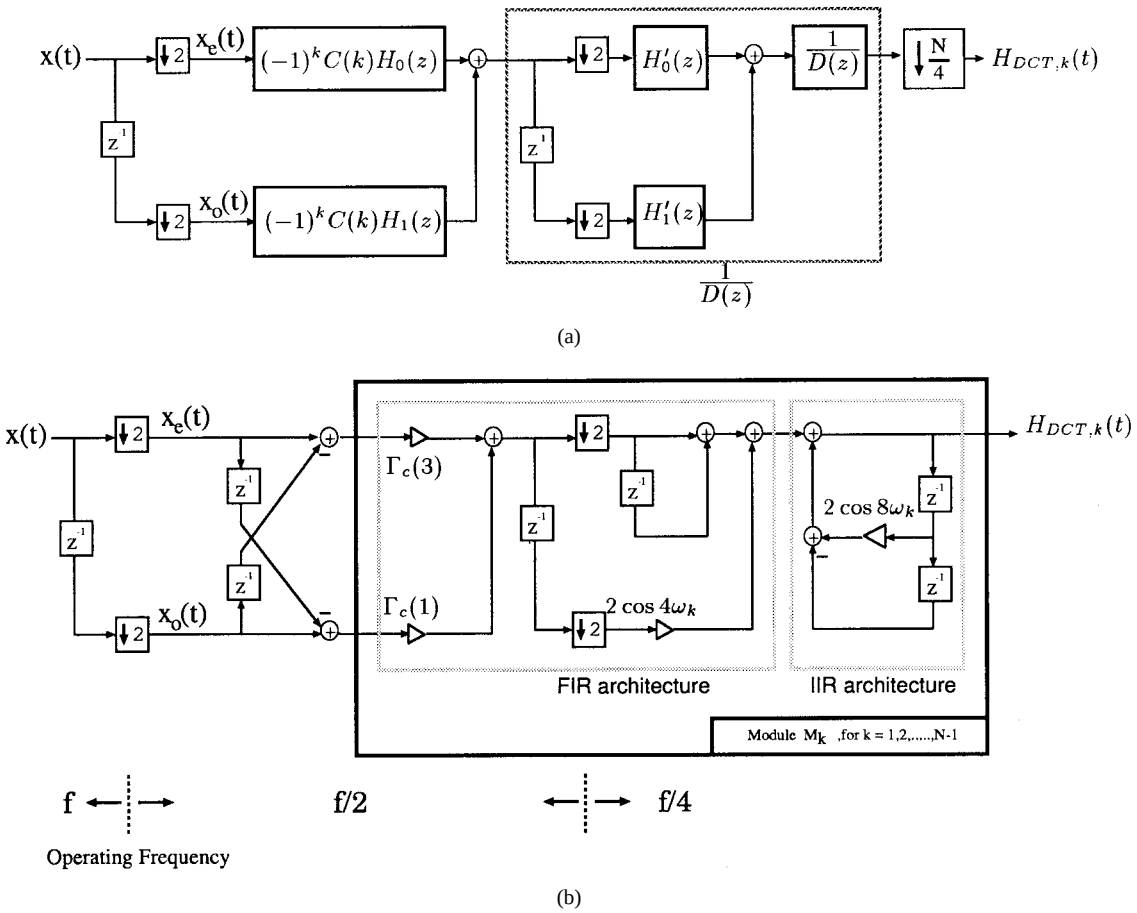

Fig. 7. (a) Polyphase representation of $H_{\mathrm{DCT},k}(z)$ in cascade form and (b) multirate DCT architecture with logarithmic complexity.

Similarly, $M = 4$ can be achieved by performing another polyphase decomposition

$$\frac{1}{D(z^2)} = \frac{H_0'(z^4) + z^{-2}H_1'(z^4)}{D'(z^4)} \tag{11}$$

with $D'(z^4) = 1 - 2\cos 8\omega_k z^{-4} + z^{-8}$, $H_0'(z^4) = 1 + z^{-4}$, and $H_1'(z^4) = 2\cos 4\omega_k$, in (10). After algebraic simplifications, we can obtain (5), and its corresponding implementation allows us to perform the DCT at four times slower clock rate. To derive the multirate transfer function with an arbitrary M, we can repeatedly apply the polyphase decomposition to the IIR transfer function until the resulting transfer function is fully expanded with all exponents being multiples of M.

D. Logarithmic Decomposition Approach

In Section II-C, we have shown that the substitution of (11) into (10) leads to the multirate DCT architecture in Fig. 4. However, this multirate design requires $O(M)$ hardware overhead to lower the input clock rate directly by four, which may not be acceptable when M is large and the chip area is limited.

In order to save the hardware complexity, we rewrite (10) together with (11) in a cascade form; i.e.,

$$H_{\mathrm{DCT},k}(z) = (-1)^k C(k) \times \left[H_0(z^2) + z^{-1}H_1(z^2)\right] \times \left[H_0'(z^4) + z^{-2}H_1'(z^4)\right] \times \frac{1}{D'(z^4)}. \tag{12}$$

Fig. 7(a) shows the polyphase implementation of (12). The corresponding cascade multirate DCT architecture is depicted in Fig. 7(b). There are two major blocks. One operates at half sample rate and the other at one-fourth sample rate. Since the denominator of the transfer function follows a special format, we can repeatedly perform the polyphase decomposition on the denominator and retain the same cascade form. We then have

$$H_{\mathrm{DCT},k}(z) = (-1)^k C(k)\left[H_0(z^2) + H_1(z^2)\right] \times \prod_{i=1}^{\log_2 M - 1} \frac{\left[\left(1 + z^{-2^{i+1}}\right) + 2z^{-2^i}\cos\left(2^{i+1}\omega_k\right)\right]}{1 - 2\cos(2M\omega_k)z^{-M} + z^{-2M}} \tag{13}$$

for $M \in 2^{Z^+}$. The resulting architecture decimates the operating frequency on a stage-by-stage base: in each stage, the operating frequency is reduced by half. After reaching the $(\log_2 M)$th stage, the clock rate becomes M times slower than the original data rate. The results can be extended to the IDCT as well as other low-power transformation designs to be discussed in next section.

E. Power Estimation and Complexity Comparison

The power dissipation in a well-designed digital CMOS circuit can be modeled as [10]

$$P \approx C_{\mathrm{eff}} \cdot V_{dd}^2 \cdot f_{\mathrm{clk}} \tag{14}$$

TABLE I
COMPARISON OF HARDWARE COST FOR THE PROPOSED LOW-POWER TRANSFORM CODING ARCHITECTURES

	Normal Operation		Downsampling by 2 ($M=2$)		Downsampling by 4 ($M=4$)	
	Multiplier	Adder	Multiplier	Adder	Multiplier	Adder
DCT	$2N-2$	$2N$	$3N-3$	$3N+1$	$5N-5$	$5N+3$
IDCT	$2N+1$	$3N$	$3N+1$	$4N+1$	$5N+1$	$6N+2$
MLT	$5N$	$5N$	$10N$	$11N$	$20N$	$23N$
ELT	$6N$	$6N$	$11N$	$12N$	$21N$	$24N$

where C_{eff} is the effective loading capacity, V_{dd} is the supply voltage, and f_{clk} is the operating frequency. Also, the lowest possible supply voltage V'_{dd} can be approximated by [1], [11]

$$\frac{V'_{dd}}{(V'_{dd}-V_t)^2} = M\frac{V_{dd}}{(V_{dd}-V_t)^2} \tag{15}$$

where M is the decimation factor and V_t is the threshold voltage of the device.

Assume that $V_{dd} = 5$ V, $V_t = 0.7$ V in the original system. From (15), it can be shown that V'_{dd} can be as low as 3.1 V for the case of $M = 2$. For the 16-point DCT under normal operation, it requires 30 multipliers and 32 adders. For the low-power 16-point DCT with $M = 2$, 45 multipliers and 49 adders are required. Provided that the capacitance due to the multipliers is dominant in the circuit and is roughly proportional to the number of multipliers, the power consumption of the low-power DCT can be estimated as

$$\left(\frac{45}{30}C_{\text{eff}}\right)\left(\frac{3.1\text{ V}}{5\text{ V}}\right)^2\left(\frac{1}{2}f\right) \approx 0.29P_0 \tag{16}$$

where P_0 denotes the power consumption of the original system. Similarly, for the case of $M = 4$, the total power of the 16-point multirate DCT can estimated as

$$\left(\frac{75}{30}C_{\text{eff}}\right)\left(\frac{2.1\text{ V}}{5\text{ V}}\right)^2\left(\frac{1}{4}f\right) \approx 0.11P_0. \tag{17}$$

Table I summarizes the hardware cost for the proposed DCT/IDCT architectures based on the polyphase decomposition approach. As we can see, we can achieve low power consumption at the expense of linear complexity overhead.

In the logarithmic low-power design, the feature of multiple operating frequencies in the logarithmic low-power architecture allows us to use different supply voltages according to the slowest allowable operating speed (the so-called voltage scaling approach). As a result, the power consumption of the 16-point low-power DCT architecture in Fig. 7(b) can be estimated as

$$\left(\frac{N_2}{N_0}C_{\text{eff}}\right)\left(\frac{3.1\text{ V}}{5\text{ V}}\right)^2\left(\frac{1}{2}f\right) + \left(\frac{N_4}{N_0}C_{\text{eff}}\right)\left(\frac{2.1\text{ V}}{5\text{ V}}\right)^2\left(\frac{1}{4}f\right) \approx 0.24P_0, \tag{18}$$

where $N_0 = 30$ is the total multipliers required in the normal DCT in Fig. 2; $N_2 = 30$ and $N_4 = 30$ are the number of multipliers in the $M = 2$ stage and $M = 4$ stage, respectively. From (18), we can see that the overall power consumption of the logarithmic low-power design is in between $M = 2$ and $M = 4$ of the full multirate DCT systems discussed in Section II-A.

As to the complexity, it can be shown that we need a total of $\log_2 M + 2$ multipliers to realize the multirate transfer function in (13). The comparison of the logarithmic low-power architecture with other approaches is listed in Table II. Although the total power saving of the logarithmic structure is less than that of the full multirate structure given the same M, the $O(\log_2 M)$ hardware overhead is preferable for low-power consumption without trading too much chip area.

F. Comparisons of Architectures

We use the DCT as an example to compare the proposed multirate SIPO architectures with well-known SIPO and PIPO architectures [3], [8]. A comparison regarding their inherent properties is listed in Table III. The advantages of the SIPO approach over the PIPO approach in their VLSI implementation, such as local communication and linear hardware complexity increase, have been discussed thoroughly in [2] and [3]. Nevertheless, when the speed compensation capability is of concern, the PIPO approach is also a good choice since the PIPO processing with block size N is equivalent to decimating the input data by a factor of N. However, this advantage is obtained at the expense of "globally" increased hardware and routing paths. Besides, the block size is usually restricted to be power of two due to the "divide-and-conquer" nature of those PIPO fast algorithms. From Table III, we can see that our multirate SIPO approach is a good compromise between the other two approaches. Basically, the multirate approach inherits all the advantages of the existing SIPO approach; meanwhile, it can compensate the speed penalty at the expense of "locally" increased hardware and routing, which is not the case in the PIPO approach.

III. UNIFIED LOW-POWER TRANSFORM CODING ARCHITECTURE

In this section, we extend the multirate design to the MLT and ELT which belong to the family of lapped orthogonal transforms (LOT) [5], [6], [12]. They can help to diminish the blocking effect encountered in low bit-rate block transforms. Then, we derive a unified transform coding architecture that is capable of performing most of the discrete orthogonal transforms based on the same VLSI computational modules.

A. The IIR MLT Structure

The MLT operating on segments of data of length $2N$, $x(t+n-2N+1)$, $n = 0, 1, \cdots, 2N-1$, is defined as [5]:

$$X_{\text{MLT},k}(t) = S(k)\sqrt{\frac{2}{N}} \times \sum_{n=0}^{2N-1} \sin\frac{\pi}{2N}\left(n+\frac{1}{2}\right) \times \cos\left[\frac{\pi}{N}\left(k+\frac{1}{2}\right)\left(n+\frac{1}{2}+\frac{N}{2}\right)\right] \times x(t+n-2N+1) \tag{19}$$

for $k = 0, 1, \cdots, N-1$, where $S(k) = (-1)^{(k+2)/2}$ if k is even, and $S(k) = (-1)^{(k-1)/2}$ if k is odd. After some

TABLE II
COMPARISON OF THE LOGARITHMIC LOW-POWER DCT ARCHITECTURE WITH OTHER APPROACHES

	Normal DCT architecture in [3]	Logarithmic low-power DCT architecture	Low-power DCT architecture in Section II-A
Multipliers	$2N-2$	$(\log M+2)N$ (in order)	$(M+1)N$ (in order)
Adders	$2N$	$(2\log M+1)N$ (in order)	$(M+1)N$ (in order)
Power consumption for 16-point DCT	P_o	$0.24P+o\ (M=4)$	$0.11P_o\ (M=4)$

TABLE III
COMPARISONS OF DIFFERENT DCT ARCHITECTURES, WHERE f_s DENOTES THE DATA SAMPLE RATE, M DENOTES THE DECIMATION FACTOR, AND N IS THE BLOCK SIZE

	Liu *et. al.* [3]	Proposed multirate IIR DCT with $M=4$	Lee [8]
Data processing rate	f_s	f_s/M	f_s/N
No. of Multipliers	$2N-2$	$(M+1)N$ (in order)	$(\frac{3N}{2})\log_2 N$ (in order)
No. of Adders	$2N$	$(M+1)N$ (in order)	$(\frac{N}{2})\log_2 N$
Latency	N	N	$[\log_2 N(\log_2 N-1)]/2$
Restriction on transform size N	No	$Mk, k\in Z^+$	$2^k, k\in Z^+$
Requirement for input buffer	No	No	Yes
Index mapping	No	No	Yes
Communication	Local	Local	Global
I/O operation	SIPO	SIPO	PIPO
Speed compensation capability	N/A	Good (at the expense of locally increased hardware overhead and local routing)	Good (at the expense of globally increased hardware overhead and global routing)
Power consumption in routing	Negligible	Negligible	Noticeable as N increases
Application to pruning DCT [21]	Direct	Direct	Needs many modifications and global interconnections

algebraic manipulations, the MLT can be decomposed into [13]

$$X_{\mathrm{MLT},k}(t) = -S(k)[X_{C,k+1}(t)+X_{S,k}(t)] \tag{20}$$

where

$$X_{C,k}(t) \triangleq \beta_1 \sum_{n=0}^{L-1} \cos[(2n+1)\omega_k+\theta_k] \times x(t+n-2N+1) \tag{21}$$

$$X_{S,k}(t) \triangleq \beta_1 \sum_{n=0}^{L-1} \sin[(2n+1)\omega_k+\theta_k] \times x(t+n-2N+1) \tag{22}$$

with block size $L=2N$, and

$$\beta_1 \triangleq \frac{1}{\sqrt{2N}},\ \omega_k \triangleq \frac{\pi k}{2N},\quad \theta_k \triangleq \frac{\pi}{2}\left(k+\frac{1}{2}\right). \tag{23}$$

The IIR transfer functions for (21) and (22) can be computed as

$$H_{C,k}(z)=\beta_1\left(1-z^{-L}\right) \times \frac{\cos\left((2L-1)\omega_k+\theta_k\right)-\cos\left((2L+1)\omega_k+\theta_k\right)z^{-1}}{1-2\cos 2\omega_k z^{-1}+z^{-2}} \tag{24}$$

$$H_{S,k}(z)=\beta_1(1-z^{-L}) \times \frac{\sin\left((2L-1)\omega_k+\theta_k\right)-\sin\left((2L+1)\omega_k+\theta_k\right)z^{-1}}{1-2\cos 2\omega_k z^{-1}+z^{-2}}. \tag{25}$$

The corresponding IIR module for the dual generation of $X_{C,k}(t)$ and $X_{S,k}(t)$ is depicted in Fig. 8(a). This IIR module can be used as a basic building block to implement MLT according to (20). Fig. 8(b) illustrates the overall time-recursive MLT architecture for the case of $N=8$. It consists of two parts: one is the *IIR module array* which computes $X_{C,k}(t)$ and $X_{S,k}(t)$ at different index k in parallel. The other is the *programmable interconnection network* which selects and combines the outputs of the IIR array to generate the MLT coefficients based on (20).

B. Low-Power Design of the MLT

As with the low-power DCT, we can compute the multirate IIR transfer functions of $H_{C,k}(z)$ and $H_{S,k}(z)$ as

$$\begin{aligned} H_{C,k}(z) =& \frac{\beta_1(1-z^{-L/2})}{1-2\cos(4\omega_k)z^{-1}+z^{-2}} \\ &\times\Big(\left[\cos\left((2L-3)\omega_k+\theta_k\right)\right. \\ &\quad \left.-\cos\left((2L+1)\omega_k+\theta_k\right)z^{-1}\right]X_e(z) \\ &+\left[\cos\left((2L-1)\omega_k+\theta_k\right)\right. \\ &\quad \left.-\cos\left((2L+3)\omega_k+\theta_k\right)z^{-1}\right]X_o(z)\Big) \end{aligned} \tag{26}$$

and

$$\begin{aligned} H_{S,k}(z) =& \frac{\beta_1(1-z^{-L/2})}{1-2\cos(4\omega_k)z^{-1}+z^{-2}} \\ &\times\Big(\left[\sin\left((2L-3)\omega_k+\theta_k\right)\right. \\ &\quad \left.-\sin\left((2L+1)\omega_k+\theta_k\right)z^{-1}\right]X_e(z) \\ &+\left[\sin\left((2L-1)\omega_k+\theta_k\right)\right. \\ &\quad \left.-\sin\left((2L+3)\omega_k+\theta_k\right)z^{-1}\right]X_o(z)\Big). \end{aligned} \tag{27}$$

The parallel architecture to realize (26) and (27) is shown in Fig. 9. It consists of two MLT modules in Fig. 8(a). Through

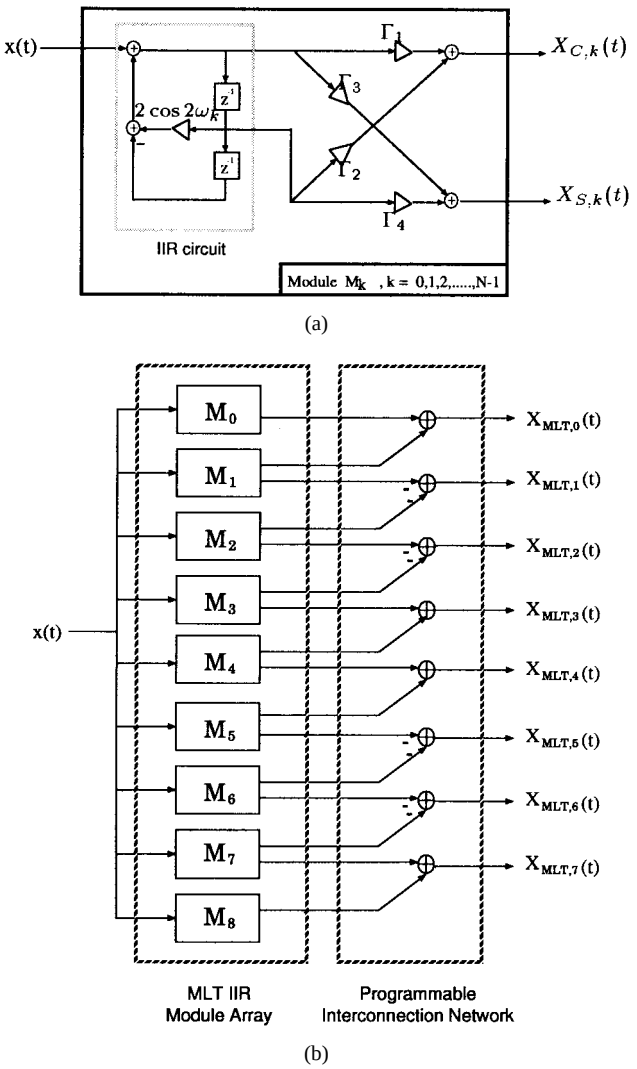

Fig. 8. (a) IIR MLT module, where $\Gamma_1 = \beta_1(\cos(2L-1)\omega_k + \theta_k)$, $\Gamma_2 = -\beta_1\cos((2L+1)\omega_k + \theta_k)$, $\Gamma_3 = \beta_1\sin((2L-1)\omega_k + \theta_k)$, $\Gamma_4 = -\beta_1\sin((2L+1)\omega_k + \theta_k)$ and (b) the time-recursive MLT architecture.

such manipulation, only decimated sequences are processed inside the module. Hence, the MLT module can operate at half of the original clock rate by doubling the hardware complexity. The comparison of hardware cost is shown in Table I. Suppose that P_0 denotes the power consumption of the MLT module in Fig. 8(a). From the CMOS power model, it can be shown that the power consumption for the low-power MLT modules is reduced to $0.38P_0$ and $0.17P_0$ for the case of $M = 2$ and $M = 4$, respectively.

C. The ELT and Unified IIR Transform Coding Design

The ELT with basis length equal to $4N$ for data segment $x(t+n-4N+1)$, $n = 0, 1, \cdots, 4N-1$, is defined as [14]

$$X_{\mathrm{ELT},k}(t) = \sqrt{\frac{2}{N}}\sum_{n=0}^{4N-1}\left[\frac{1}{2\sqrt{2}} - \frac{1}{2}\cos\frac{\pi}{N}\left(n+\frac{1}{2}\right)\right] \times \cos\left[\frac{\pi}{N}\left(k+\frac{1}{2}\right)\left(n+\frac{1}{2}+\frac{N}{2}\right)\right] \times x(t+n-4N+1) \quad (28)$$

for $k = 0, 1, \cdots, N-1$. As with the treatment of the MLT, we can rewrite (28) as

$$X_{\mathrm{ELT},k}(t) = -\tilde{X}_{S,k+1}(t) + \sqrt{2}\tilde{X}_{C,k}(t) + \tilde{X}_{S,k-1}(t) \quad (29)$$

where

$$\tilde{X}_{C,k}(t) \triangleq \beta_2\sum_{n=0}^{L-1}\cos[(2n+1)\omega'_k + \theta'_k] \times x(t+n-4N+1) \quad (30)$$

$$\tilde{X}_{S,k}(t) \triangleq \beta_2\sum_{n=0}^{L-1}\sin[(2n+1)\omega'_k + \theta'_k] \times x(t+n-4N+1) \quad (31)$$

with

$$L = 4N,\ \beta_2 \triangleq \frac{1}{2\sqrt{2N}},\ \omega'_k \triangleq \frac{\pi}{2N}\left(k+\frac{1}{2}\right)$$
$$\theta'_k \triangleq \frac{\pi}{2}\left(k+\frac{1}{2}\right). \quad (32)$$

Define the relationship in (20) and (29) as the *combination functions*. After comparing (20)–(23) with (29)–(32), we see that the MLT and ELT have identical mathematical structures except for the definitions of parameters and the combination functions. Hence, they can share the same VLSI architectures that are depicted in Figs. 8 and 9. We only need to change the multiplier coefficients [use (32)] and interconnection network [use (29)] to perform the ELT.

The aforementioned design concept can be generalized to perform most of existing discrete sinusoidal transforms. For example, $X_{C,k}(t)$ in (21) is equivalent to the DCT by setting

$$L = N,\ \beta_1 = C(k),\ \omega_k = \frac{k\pi}{2N},\ \theta_k = 0. \quad (33)$$

As a result, the multirate MLT module in Figs. 8 and 9 can be used to compute the DCT.

The other example is the discrete Fourier transform (DFT) with real-valued inputs. With the following parameter setting:

$$L = N,\ \beta_1 = \frac{1}{\sqrt{N}},\ \omega_k = \frac{-k\pi}{N},\ \theta_k = -\omega_k \quad (34)$$

(21) and (22) become

$$XC,k(t) = \frac{1}{\sqrt{N}}\sum_{n=0}^{N-1}\cos\left(\frac{-2\pi}{N}kn\right)x(t+n-N+1) \quad (35)$$

$$X_{S,k}(t) = \frac{1}{\sqrt{N}}\sum_{n=0}^{N-1}\sin\left(\frac{-2\pi}{N}kn\right)x(t+n-N+1) \quad (36)$$

which are the real part and the imaginary part of the DFT, respectively. The setting of parameters as well as the corresponding combination functions for other orthogonal transforms is summarized in Table IV. The programmable feature of the unified transform coding architecture can be incorporated into the design of a high-performance reconfigurable DSP computing engine for multimedia applications [15].

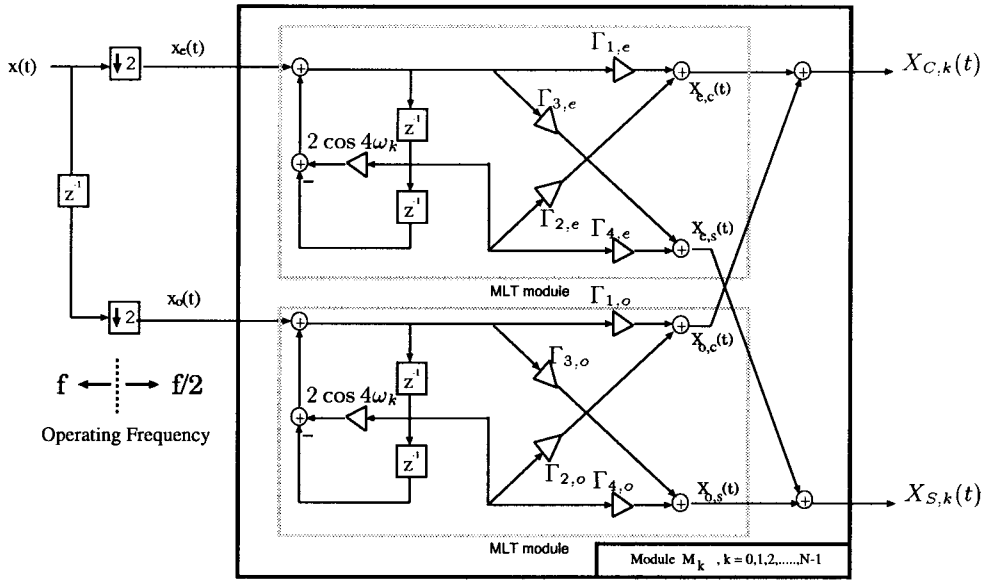

Fig. 9. Low-power IIR MLT module design, where $\Gamma_{1,e} = \beta_1 \cos((2L-3)\omega_k+\theta_k)$, $\Gamma_{2,e} = -\beta_1 \cos((2L+1)\omega_k+\theta_k)$, $\Gamma_{3,e} = \beta_1 \sin((2L-3)\omega_k+\theta_k)$, $\Gamma_{4,e} = -\beta_1 \sin((2L+1)\omega_k+\theta_k)$, $\Gamma_{1,o} = \beta_1 \cos((2L-1)\omega_k+\theta_k)$, $\Gamma_{2,o} = -\beta_1 \cos((2L+3)\omega_k+\theta_k)$, $\Gamma_{3,o} = \beta_1 \sin((2L-1)\omega_k+\theta_k)$, $\Gamma_{4,o} = -\beta_1 \sin((2L+3)\omega_k+\theta_k)$.

TABLE IV
PARAMETER SETTING FOR THE UNIFIED LOW-POWER IIR TRANSFORMATION ARCHITECTURE

	L	β_1	ω_k	θ_k	Combination Function
DCT	N	$C(k)$	$\frac{k\pi}{2N}$	0	$X_{DCT,k}(t) = X_{C,k}(t)$
IDCT	N	$C(1)$	$\frac{\pi}{2N}(k+\frac{1}{2})$	$-\omega_k$	$X_{IDCT,k}(t) = X_{C,k}(t) + (C(0)-C(1))x(n-N+1)$
DST-IV in [22]	N	$C(1)$	$\frac{\pi}{2N}(k+\frac{1}{2})$	0	$X_{DST,k}(t) = X_{S,k}(t)$
IDST-IV in [22]	N	$C(1)$	$\frac{\pi}{2N}(k+\frac{1}{2})$	0	$X_{IDST,k}(t) = X_{S,k}(t)$
MLT	$2N$	$\frac{1}{\sqrt{2N}}$	$\frac{k\pi}{2N}$	$\frac{\pi}{2}(k+\frac{1}{2})$	$X_{MLT,k}(t) = -S(k)[\,X_{C,k+1}(t) + X_{S,k}(t)\,]$
ELT	$4N$	$\frac{1}{2\sqrt{2N}}$	$\frac{\pi}{2N}(k+\frac{1}{2})$	$\frac{\pi}{2}(k+\frac{1}{2})$	$X_{ELT,k}(t) = -X_{S,k+1}(t) + \sqrt{2}X_{C,k}(t) + X_{S,k-1}(t)$
DFT	N	$\frac{1}{\sqrt{N}}$	$-\frac{k\pi}{N}$	$-\omega_k$	$Re\{X_{DFT,k}(t)\} = X_{C,k}(t),\ Im\{X_{DFT,k}(t)\} = X_{S,k}(t).$
DHT	N	$\frac{1}{\sqrt{N}}$	$-\frac{k\pi}{N}$	$-\omega_k$	$X_{DHT,k}(t) = X_{C,k}(t) + X_{S,k}(t).$

IV. FINITE-PRECISION ANALYSIS

In this section, we consider the finite-precision effects of the proposed low-power DCT architectures. There are two basic considerations in the fixed-point analysis. One is the *rounding error*. The mean and variance of the rounding error are given by [16, ch. 6]

$$m_R = 0,\ \sigma_R^2 = \frac{2^{-2B}}{12} \tag{37}$$

respectively, where B is the assigned wordlength. The other is the *dynamic range*. To prevent overflow in fixed-point implementation, a suitable scaling of the input signal is usually employed according to the dynamic range of the system. In practice, the SNR of the scaled system, SNR′, will be degraded by the scaling process and is given by [16, ch. 6]

$$\text{SNR}' = s^2\text{SNR}_0 \tag{38}$$

where s is the scaling factor, and SNR_0 is the SNR of the original system.

A. Analysis for the Normal IIR DCT

Using the "statistical error model" [16, ch. 6], the rounding error of the IIR DCT structure in Fig. 2 can be modeled as

$$e(t) = e_1(t) + e_2(t) \tag{39}$$

where $e_i(t)$ is the rounding error caused by the ith multiplier. It can be shown that

$$m_e = E\{e(t)\} = 0,\ \sigma_e^2 = E\{e^2(t)\} = \big(1 + N_s(k)\big)\cdot\sigma_R^2 \tag{40}$$

where $N_s(k)$ is the number of the noise sources contributed by the multiplier in the IIR loop:

$$N_s(k) = \begin{cases} 4, & \text{if } |2\cos(2\omega_k)| > 1 \\ 1, & \text{if } |2\cos(2\omega_k)| < 1 \\ 0, & \text{if } |2\cos(2\omega_k)| = 1. \end{cases} \tag{41}$$

Due to the presence of $e(t)$, the actual output of the DCT architecture can be represented as

$$\hat{X}_{\text{DCT},k}(t) = X_{\text{DCT},k}(t) + f(t) \tag{42}$$

where $f(t)$ is the output error contributed by $e(t)$. Let $H_{ef}(z)$ denote the transfer function of the system from the node

at which $e(t)$ is injected to the output, and $h_{ef}(n)$ be the corresponding unit-sample response. From Fig. 2, it can be shown that $H_{ef}(z) = 1/(1 - 2\cos 2\omega_k z^{-1} + z^{-2})$, and

$$h_{ef}(n) = \frac{1}{\sin(2\omega_k)} \sin[(n+1)2\omega_k]. \tag{43}$$

Since only N iterations are performed in the IIR structure, we have

$$m_f = E\{f(t)\} = m_e \sum_{n=0}^{N-1} h_{ef}(n) = 0 \tag{44}$$

$$\sigma_f^2 = E\{f^2(t)\} = \sigma_e^2 \sum_{n=0}^{N-1} |h_{ef}(n)|^2 = \frac{\sigma_e^2}{\sin^2(2\omega_k)}\left(\frac{N}{2}\right). \tag{45}$$

Based on (40)–(45), we can represent the total noise power at the kth DCT channel as

$$P_f = m_f^2 + \sigma_f^2 = \frac{N(N_s(k)+1)}{2\sin^2(2\omega_k)}\left(\frac{2^{-2B_k}}{12}\right). \tag{46}$$

As we can see, given the channel wordlength B_k, the rounding error grows linearly with the block size N. On the other hand, the noise power is inversely proportional to $\sin^2(2\omega_k)$. That is, the effect of the rounding error in each channel of the IIR DCT greatly depends on the pole locations of the IIR transfer function.

Next, we consider the dynamic range. By examining those nodes in Fig. 2 that may cause overflow, the dynamic range (D) of the overall IIR DCT structure can be found to be

$$D = \max\left\{2, C(k) \sum_{n=0}^{N-1} |\cos[(2n+1)\omega_k]|\right\}. \tag{47}$$

Suppose that a one-time scaling scheme is used at the input end to avoid overflow, and it is done by shifting the data to the right by K bits. The scaling factor s can be represented as

$$s = \frac{1}{2^K}, \quad \text{with} \quad K = \lceil \log_2 D \rceil. \tag{48}$$

Assume that the input sequence $x(t)$ is uniformly distributed over $(-1, 1)$ with zero mean. From (38), (46), and (48), we have

$$\text{SNR}' = s^2 \frac{E\left\{\left(X_{\text{DCT},k}(t)\right)^2\right\}}{P_f} = \frac{8\sin^2(2\omega_k)}{N(N_s(k)+1)} \cdot 2^{2B_k - 2K} \tag{49}$$

where the fact that $E\{(X_{\text{DCT},k}(t))^2\} = 1/3$, is used [17]. To achieve 40 dB in SNR for the kth DCT channel, the optimal wordlength B_k can be computed as

$$B_k = \left\lceil \frac{4 - \log_{10}\left[\sin^2(2\omega_k) \cdot \dfrac{8}{N(N_s(k)+1)}\right]}{2 \cdot \log_{10} 2} + K \right\rceil. \tag{50}$$

As an example, the B_k's for the case $N = 8$ under the constraint SNR = 40 dB are listed in Table V, where B_A denotes the averaged system wordlength. As we can see, $B_A = 11$ bits is sufficient to meet the accuracy criteria. Compared with the DCT implementations in [18] and [19], in which B_A was chosen based on the experimental simulation results, our analytical approach provides more insightful information to determine the architectural specification than the experimental approach.

TABLE V
OPTIMAL WORDLENGTH ASSIGNMENT UNDER THE CONSTRAINT SNR = 40 dB, WHERE $N = 8$

DCT channel k	1	2	3	4	5	6	7	B_A
B_k $(Normal)$	12	11	10	9	10	11	12	10.7
B_k $(Multirate\ with\ M = 2)$	10	9	10	11	10	9	10	9.9

B. Analysis for the Low-Power IIR DCT with $M = 2$

In Fig. 3, the power of the injected rounding error can be modeled as

$$\sigma_e^2 = E\{e^2(t)\} = (2 + N_s(k))\sigma_R^2. \tag{51}$$

Note that $H_{ef}(z) = 1/(1 - 2\cos 4\omega_k z^{-1} + z^{-2})$, and the total iteration is reduced to $N/2$. The total noise power at the output becomes

$$\sigma_f^2 = \sigma_e^2 \sum_{n=0}^{N/2-1} |h_{ef}(n)|^2 = \frac{\sigma_e^2}{\sin^2(4\omega_k)}\left(\frac{N}{4}\right) = \frac{(2 + N_s(k))N\sigma_R^2}{4\sin^2(4\omega_k)}. \tag{52}$$

From (52), we observe the following.

1) Although the total number of noise sources increases, the total noise power is compensated by the halved number of iterations.
2) Compared with the factor $1/(\sin(2\omega_k)^2)$ in (46), the factor $1/(\sin(4\omega_k)^2)$ in (52) will have similar effect on the SNR of each DCT channel but with halved period.

Next we apply the technique of "superimposition" to analyze the dynamic range of the multirate DCT architecture. Namely, we first set $x_o(t)$ to zero while analyzing the dynamic range contributed by $x_e(t)$; then we perform the same analysis for $x_o(t)$ by setting $x_e(t)$ to zero. The overall D can be found from the summation of the two dynamic ranges, which is given by

$$D_1 = 2C(k)(|\cos\omega_k| + |\cos 3\omega_k|),$$
$$D_2 = C(k) \sum_{n=0}^{N/2-1} (|\cos[(4n+1)\omega_k]| + |\cos[(4n+3)\omega_k]|),$$
$$D = \max\{D_1, D_2\}. \tag{53}$$

Using the analytical results in (52) and (53), we can also find the optimal wordlengths for $N = 8$ under the 40-dB SNR constraint as shown in Table V. It is interesting to note that the multirate DCT architecture can not only achieve low-power consumption, its numerical property under fixed-point implementation is also better than the normal DCT architecture.

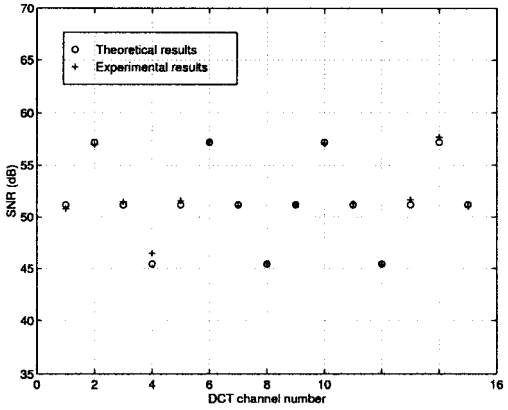

Fig. 10. Average SNR as a function of DCT channel number under fixed-point arithmetic ($N = 16$, $B = 12$, $M = 4$).

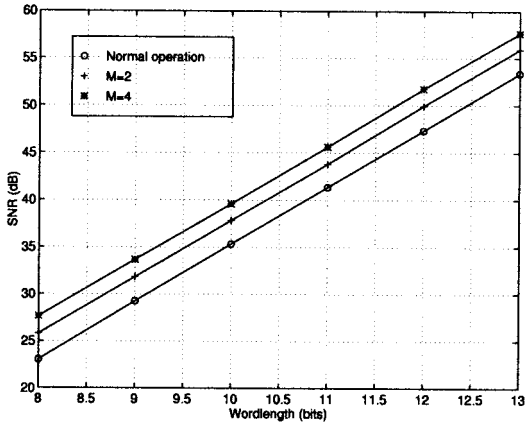

Fig. 11. Average SNR as a function of wordlength under fixed-point arithmetic ($N = 16$). The multirate low-power architectures have better SNR as M increases.

The above analyses can be extended to low-power DCT designs with decimation factor $M \geq 2$, $M \in 2^{+Z}$. The results are given by

$$P_f = (M + N_s(k))\left(\frac{N}{2^{m+1}}\right)\frac{\sigma_R^2}{\sin^2(2^{m+1}\omega_k)} \tag{54}$$

$$D_1 = M \cdot C(k) \sum_{n=0}^{M-1} |\cos[(2n+1)\omega_k]|$$

$$D_2 = C(k) \sum_{n=0}^{(N/M)-1} \sum_{i=0}^{M-1} |\cos[(2^{m+1}n + 2i + 1)\omega_k]|$$

$$D = \max\{D_1, D_2\} \tag{55}$$

with $m = \log_2 M$. To verify our analytical results, computer simulations are carried out. As we can see in Fig. 10, there is a close agreement between the theoretical and experimental results. Also, the SNR distribution is affected by the factor $\sin^2(2^{m+1}\omega_k)$ in (54).

Fig. 11 shows the averaged SNR for $N = 16$. Compared with the simulation results in [17], the proposed IIR DCT architectures give comparative SNR performance to the DCT architectures by Hou [7] and Lee [8] under fixed-point arithmetic. It is worth noting that the multirate DCT architectures have better SNR results than the normal IIR DCT architectures.

V. Conclusions

In this paper, we presented the algorithm-based low-power design of the transform coding kernels using multirate approach. Extension of our designs to low-power 2-D transforms can be achieved by employing the time-recursive 2-D DCT architecture proposed by Chiu and Liu [20]. Another attractive application of our design is in the very high-speed data processing. Suppose that we do not lower the supply voltage for low power consumption. The multirate parallel architectures are in fact high-speed VLSI architectures with speedup of M. For example, if we want to perform DCT for serial data at 200 MHz, we may use the parallel architecture in Fig. 4, in which only 50 MHz adders and multipliers are required. Therefore, we can perform very high-speed DCT by using only low-cost and low-speed processing elements.

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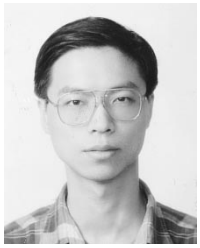

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